# FAN7680

## PC Power Supply Outputs Monitoring IC

### Features

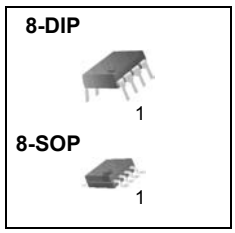
- PC Power Supply Output Monitor Circuitry
- Few External Components
- Over Voltage Protection for 3.3V, 5V and 12V(Vcc) Outputs
- Under Voltage Protection for 3.3V, 5V and 12V(Vcc) Outputs with Delay Time
- Fault Protection Output with Open Drain Output
- Open Drain Power Good Output
- 300ms Power Good Delay
- 38ms $\overline{\text{PSON}}$ On/Off Debounce
- 73us Debounce
- 2.3ms $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$ Turn Off Delay
- Latch Function Controlled by $\overline{\text{PSON}}$ and Protection Inputs

### Typical Application

- PC Power Supply

### Description

The FAN7680 is a complete output supervisory circuitry intended for use in the secondary side of a switched mode power supply. It provides over voltage protection (OVP), under voltage protection (UVP), fault protection output ($\overline{\text{FPO}}$), remote On/Off ($\overline{\text{PSON}}$), latch, internal delay circuits and power good signal generator to monitor and control the output of the switching power supply system. As for output control, power good output(PGO) and fault protection output($\overline{\text{FPO}}$) are included. It directly senses all the output rails for OVP and UVP without external dividers. The FAN7680 offers a simple and cost effective solution with minimum number of external components and greatly reduces PCB board space for power supply.




#### OVP

The FAN7680 has OVP functions for +3.3V, +5V, +12V(Vcc) outputs. This block is made up of three comparators with two inputs and resistor dividers. One input of a comparator is connected to a reference voltage and another input is connected to a resistor divider.

#### UVP

The FAN7680 also has UVP functions for +3.3V, +5V, +12V(Vcc) outputs. This block is made up of three comparators with two inputs and resistor dividers. One input of a comparator is connected to a reference voltage and another input is connected to a resistor divider.

#### $\overline{\text{PSON}}$

The remote on/off($\overline{\text{PSON}}$) section is for controlling the SMPS externally. When a high signal is applied to the $\overline{\text{PSON}}$ input, the $\overline{\text{FPO}}$ signal becomes a high state and all secondary outputs are grounded. The remote on/off signal is transferred with some on/off debounce time.

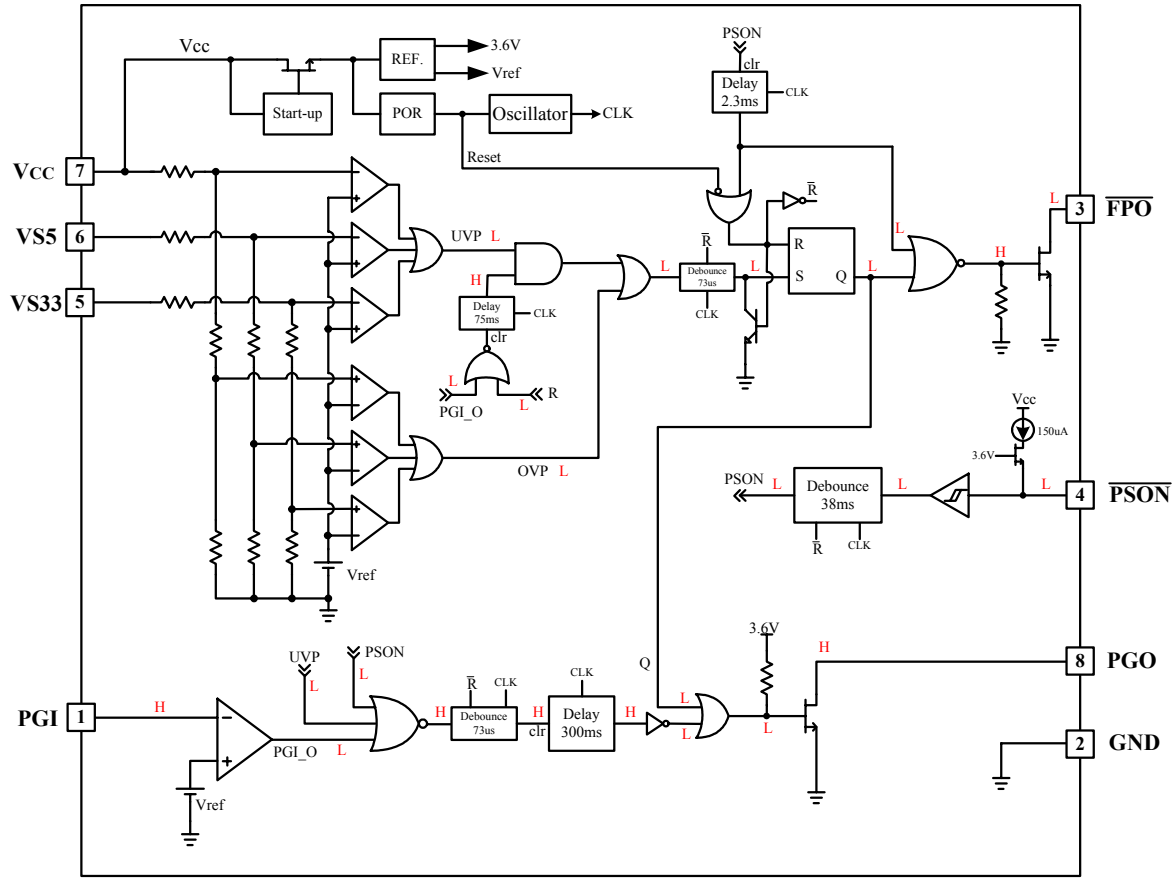
#### $\overline{\text{FPO}}$

The $\overline{\text{FPO}}$(Fault Protection Output) is a signal which indicates the system fault condition according to protection signals. When a fault state is occured, the $\overline{\text{FPO}}$ signal becomes high and the PGO signal becomes low and the main power is to be turned off.
Normal State; "Low"
Fault State; "High"

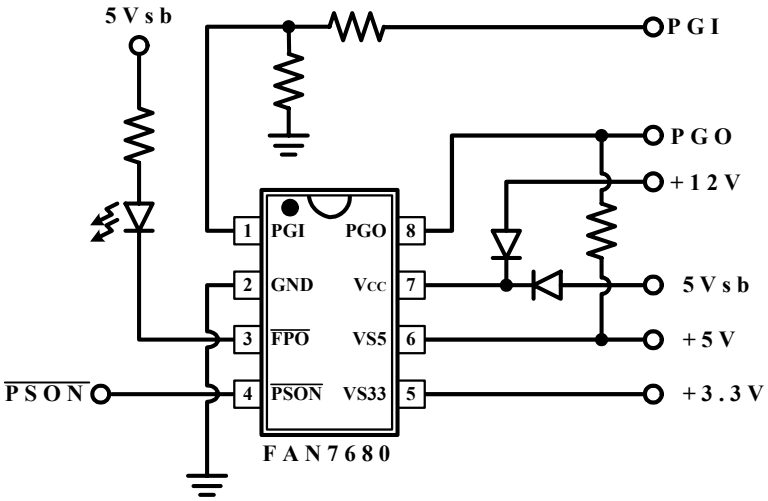
#### PGO

The power good signal generator provides a signal according to output voltage conditions of a power supply for safe operation of a secondary system. The power good output should be low state before the output voltage is out of regulation at turn-off of the input power switch.
Normal State ; "High"
Fault State ; "Low"

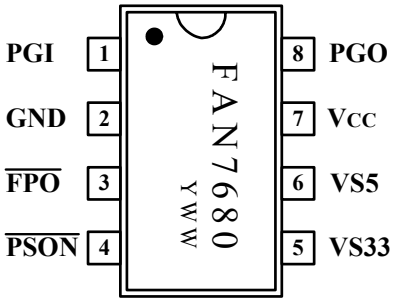
## Internal Block Diagram




## Typical Applicatin Circuit



## Pin Assignments




YWW :Work Week Code

## Pin Definitions

| Pin Number | Pin Name | I/O | Pin Function Description |
|---|---|---|---|
| 1 | PGI | I | Power Good Input |
| 2 | GND | - | Ground |
| 3 | $\overline{\text{FPO}}$ | O | Low Active Fault Protection Output, Open Drain Output Stage |
| 4 | $\overline{\text{PSON}}$ | I | Remote On/Off Control Input |
| 5 | VS33 | I | 3.3V Output Voltage Input |
| 6 | VS5 | I | 5V Output Voltage Input |
| 7 | $V_{CC}$ | I | Supply Voltage and 12V Output Voltage Input |
| 8 | PGO | O | Power Good Output Signal |

## Absolute Maximum Ratings (Note2,3)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 16 | V |
| Supply Current | $I_{CC}$ | 1 | mA |
| Input Voltage | $V_{\overline{PSON}}$, VS5 | 8 | V |
| | VS33, $V_{PGI}$ | | |
| Output Voltage | $V_{PGO}$ | 8 | V |
| | $V_{\overline{FPO}}$ | 16 | |
| Operating Temperature | $T_O$ | -40 ~ +125 | °C |
| Storage Temperature | $T_S$ | -65 ~ +150 | °C |
| Power Dissipation | $P_D$ | 1 | W |

## Recommended Operating Conditions (Note2,3)

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | | 4 | | 15 | V |
| Input Voltage | $V_{\overline{PSON}}$ , VS5, | | | | 7 | V |
| | VS33, $V_{PGI}$ | | | | | |
| Output Voltage | $V_{PGO}$ | | | | 7 | V |
| | $V_{\overline{FPO}}$ | | | | 15 | V |
| Output Sink Current | $I_{\overline{FPO}}$ | | | | 30 | mA |
| | $I_{PGO}$ | | | | 10 | mA |
| Supply Voltage Rising Time | tr | Note1 | 1 | | | ms |

## Electrical Characteristics

($V_{CC}$ = 5V, Ta=25°C, unless otherwise specified)

### Over Voltage Protection, Under Voltage Protection and $\overline{FPO}$

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Over Voltage Threshold | $VS33_{OV}$ | | 3.9 | 4.1 | 4.3 | V |
| | $VS5_{OV}$ | | 5.8 | 6.1 | 6.4 | |
| | $12V(V_{CC})_{OV}$ | | 13.3 | 13.8 | 14.3 | |
| Under Voltage Threshold | $VS33_{UV}$ | | 2.55 | 2.69 | 2.83 | V |
| | $VS5_{UV}$ | | 4.1 | 4.3 | 4.5 | |
| | $12V(V_{CC})_{UV}$ | | 8.8 | 9.3 | 9.8 | |
| Leakage Current($\overline{FPO}$) | $I_{LKG1}$ | $V_{\overline{FPO}}$ = 5V | - | - | 5 | uA |
| Low Level Output Voltage($\overline{FPO}$) | $V_{OLI}$ | Isink=10mA | - | - | 0.3 | V |
| | | Isink=30mA | - | - | 0.7 | |

### PGI and PGO

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Threshold Voltage(PGI) | $V_{PGI}$ | | 1.16 | 1.20 | 1.24 | V |
| Leakage Current(PGO) | $I_{LKG2}$ | $V_{PGO}$ = 5V | - | - | 5 | uA |
| Low Level Output Voltage(PGO) | $V_{OL2}$ | Isink=10mA | - | - | 0.4 | V |

### $\overline{PSON}$ Control

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Pull-up Current | | $V_{\overline{PSON}}$ = 0V | - | 150 | - | uA |
| High-Level Input Voltage | | | 2.4 | - | - | V |
| Low-Level Input Voltage | | | - | - | 1.2 | V |

### Total Device

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Current | $I_{CC}$ | $V_{\overline{PSON}}$ = 5V | - | - | 1 | mA |

## Timing Characteristics

($V_{CC}$=5V, Ta=25°C, unless otherwise specified)

| Characteristic | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Debounce Time($\overline{PSON}$) | $t_{b1}$ | | 25 | 38 | 51 | ms |
| Noise Debounce Time | $t_{b2}$ | Note 4 | 50 | 73 | 100 | us |
| PGO Delay Time(PGI to PGO) | $t_{d1}$ | | 200 | 300 | 410 | ms |
| Internal UVP Delay Time | $t_{d2}$ | $\overline{FPO}$ goes low and every time PGI > 1.20 | 51 | 75 | 102 | ms |
| $\overline{PSON}$ Off to $\overline{FPO}$ Delay Time | $t_{d3}$ | | $t_{b1}$+1.6 | $t_{b1}$+2.3 | $t_{b1}$+3.2 | ms |

**Note**

1. $V_{CC}$ slew rate must be less than 14V/ms.
2. All voltages are measured with respect to the ground pin, unless otherwise specified.
3. The Absolute Maximum Ratings indicate the limits that if exceed, damage to the device may occur. Recommended Operating Conditions indicate conditions in which the device is functional, but do not guarantee specific performance limits.
4. This parameter, although guaranteed over the Timing Characteristics, is not 100% tested in production.

# Typical Characteristics

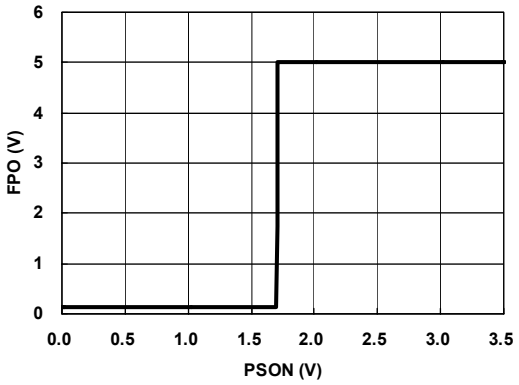



Figure 1. $\overline{\text{PSON}}$ Threshold Voltage

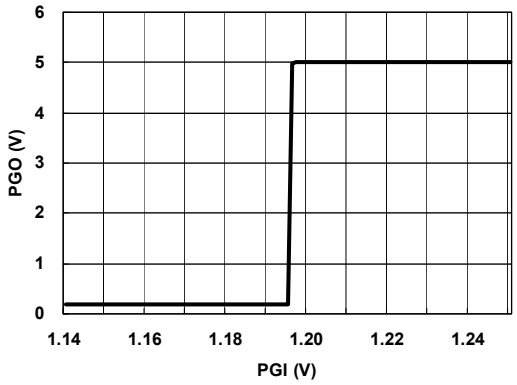



Figure 2. PGI Threshold Voltage

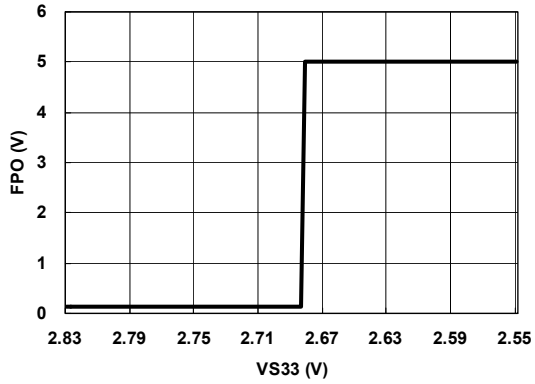



Figure 3. +3.3V UVP Voltage

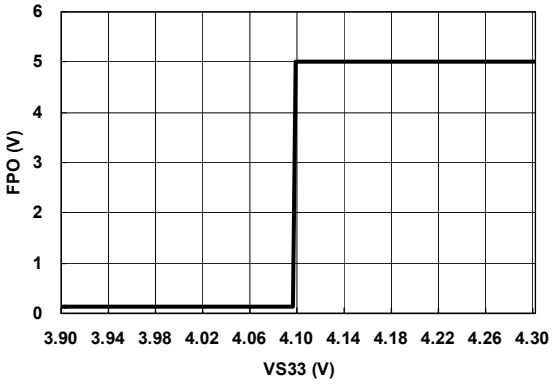



Figure 4. +3.3V OVP Voltage

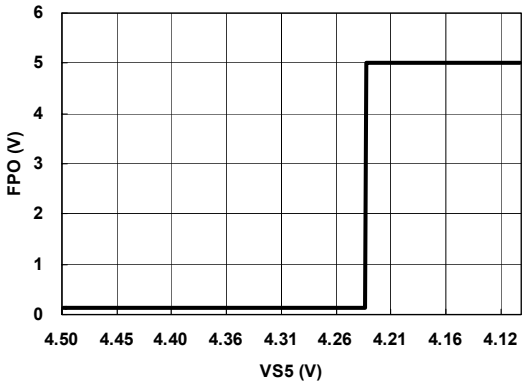



Figure 5. +5V UVP Voltage

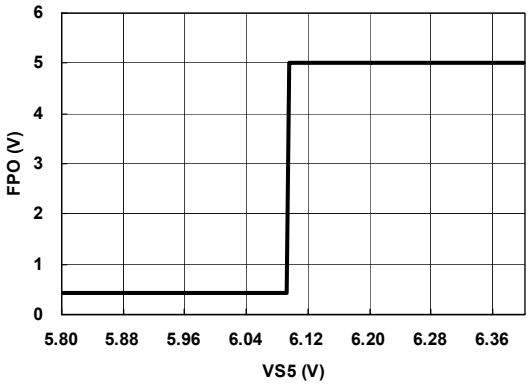



Figure 6. +5V OVP Voltage

## Typical Characteristics

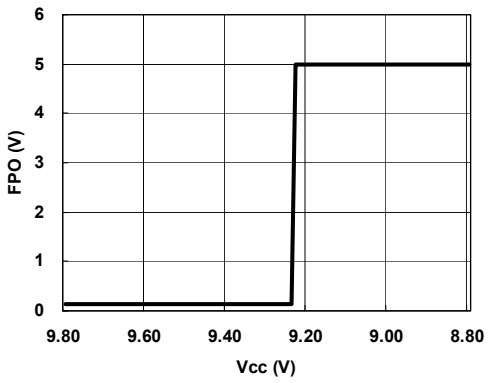



Figure 7. +12V UVP Voltage

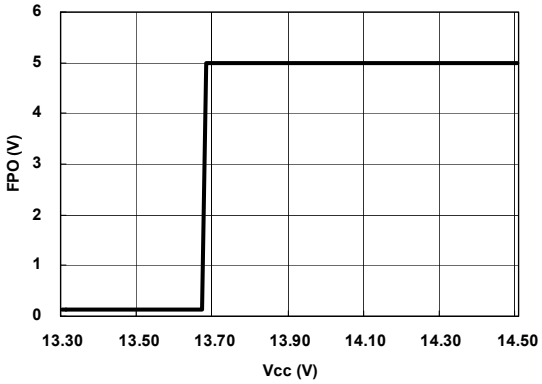
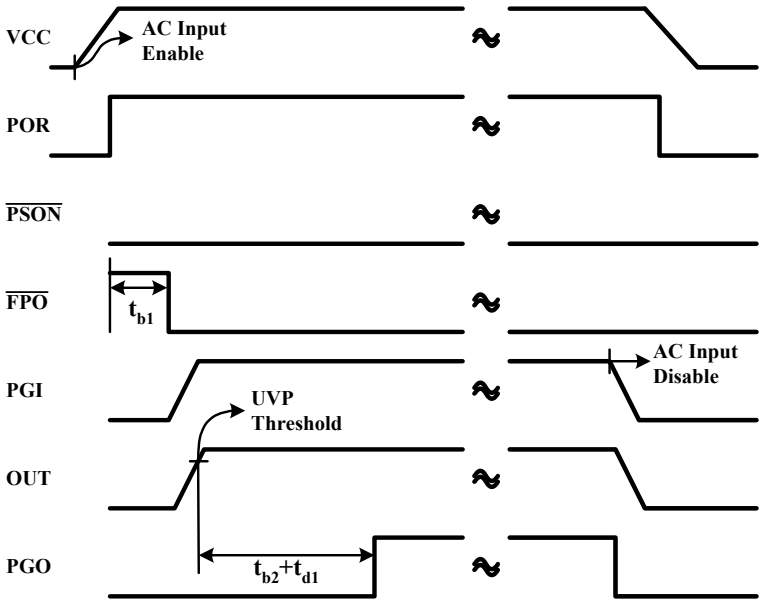


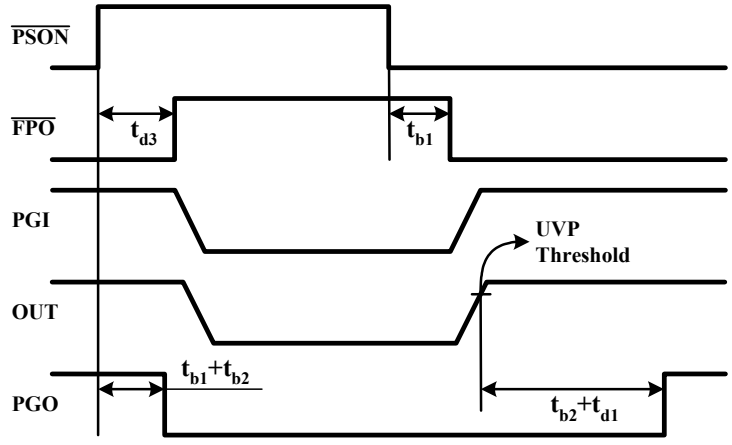

Figure 8. +12V OVP Voltage

# Timing Chart

## 1) AC Input ON/OFF - Normal State

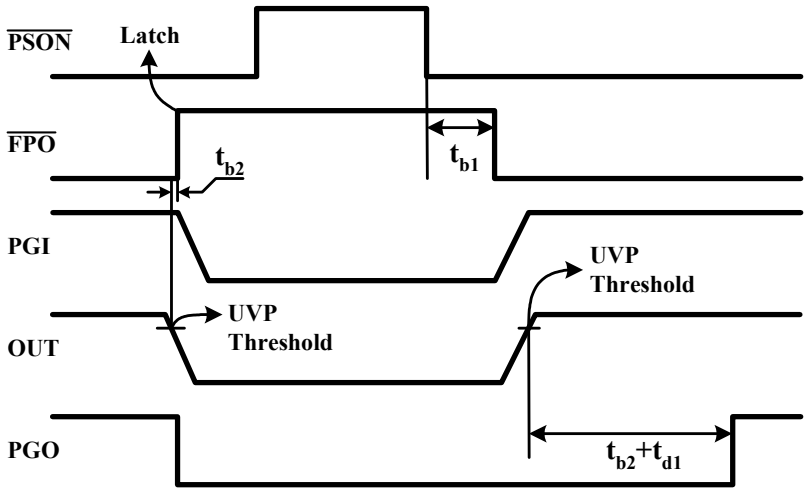



## 2) $\overline{\text{PSON}}$ ON/OFF - Normal State

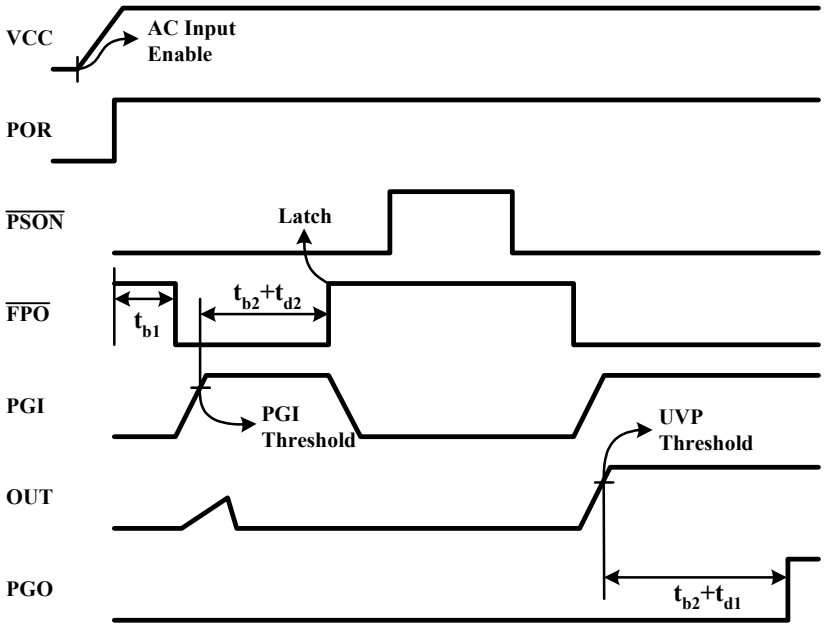



- Vcc : Supply Voltage
- POR : Power On Reset
- $\overline{\text{PSON}}$ : Power Supply On/Off
- $\overline{\text{FPO}}$ : Fault Protection Output
- PGI : Power Good Input
- OUT : Output Voltages
- PGO : Power Goood Output

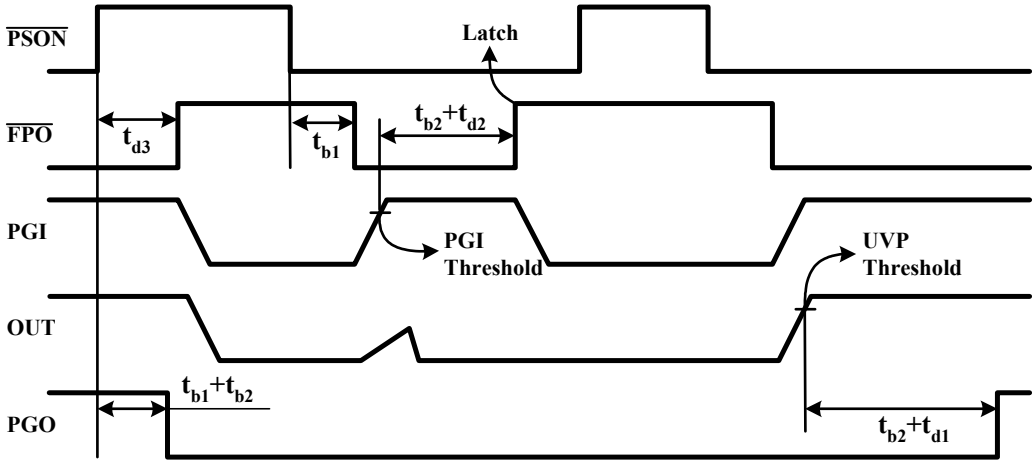
### 3) Under Voltage at Normal State



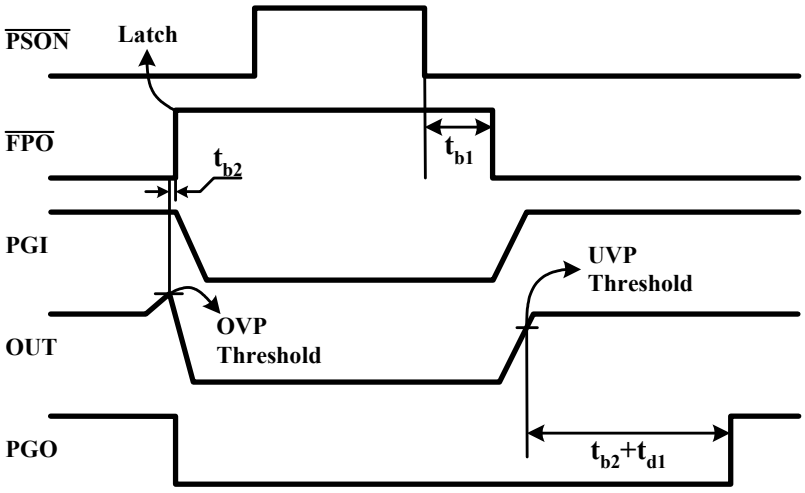

### 4) Under Voltage at AC Input ON



### 5) Under Voltage at $\overline{\text{PSON}}$ ON/OFF




### 6) Over Voltage at $\overline{\text{PSON}}$ ON/OFF



# Application Information

## Power Good(PGO) and Power Good Delay

A PC power supply is commonly designed to provide the motherboard with a power good signal, which is defined by the computer manufactures. If the +3.3V, +5V, and +12V outputs are above the undervoltage threshold limit, the PC power supply makes the power good signal high after some delay. At this time the power supply should be able to provide enough power to assure continuous operation within the specification. Conversely, when one of the +3.3V, +5V, or +12V outputs falls below the undervoltage threshold or rise above the overvoltage threshold, or when main power has been turned off for a sufficiently long time so that power supply operation is no longer assured, a PGO signal will be a low state.

The AC input, power good(PGO), remote on/off($\overline{\text{PSON}}$), and +3.3V/+5V/+12V supply rails are shown in figure 1.

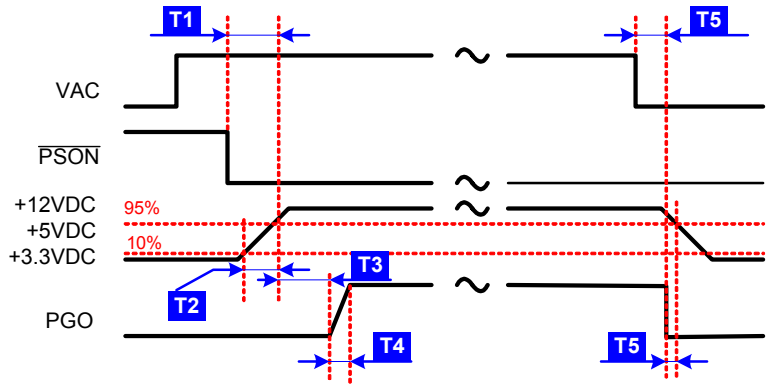



**Figure 1. Timing Diagram**

Although there is no requirement for specific timing parameters, the following signal timings are recommended :

-T1(Power On Time) : T1 < 500ms
-T2(Rise Time) : 0.1ms ≤ T2 ≤ 20ms
-T3(PGO Delay) : 100ms < T3 <500ms
-T4(PGO Delay Risetime) : T4 ≤ 10ms
-T5(AC Loss to PGO Hold-Up Time) : T5 ≥ 16ms
-T6(Power Down Warning) : T6 ≥ 1ms

Furthermore, motherboards should be designed to comply with the above recommended timing range. If timings other than these are implemented or required, that information should be clearly specified.

The FAN7680 provides a power good(PGO) signal for the +3.3V, +5V and +12V(Vcc) supply voltage rails and a separate power good input(PGI). An internal delay circuit is used to generate a 300ms power good delay.

If voltages at PGI(+1.2V), VS33(+3.3V), VS5(+5V), and Vcc(+12V) rise above the undervoltage threshold, the open drain power good output(PGO) will go high after a delay of 300ms. When the PGI voltage or any of +3.3V, +5V, and +12V rails drops below the undervoltage threshold, the PGO signal will be disabled immediately.

## Power Supply Remote On/Off($\overline{\text{PSON}}$) and Fault Protect Output($\overline{\text{FPO}}$)

Since the latest personal computer generation focuses on easy turn on and power saving functions, a PC power supply will require two characteristics. One is a dc power supply remote on/off function; the other is standby voltage to achieve very low power consumption of the PC power supply. Thus, the main power needs to be shut down.

The power supply remote on/off($\overline{\text{PSON}}$) is an active-low signal that turns on all of the main power rails including the +3.3V, +5V, and +12V power rails. When this signal is held high by the PC motherboard or left open circuited, the signal of the fault protect output($\overline{\text{FPO}}$) also goes high. Thus, the main power rails can not deliver power and are held at 0V.

When the $\overline{\text{FPO}}$ signal is held high due to an fault condition, the fault status will be latched and the outputs of the main power rails can not deliver power and are held at 0V. Toggling the $\overline{\text{PSON}}$ input signal from low to high will reset the fault protection latch. During this fault condition only the standby power is not affected.

When the $\overline{\text{PSON}}$ input signal goes from high to low or low to high, the 38ms debounce block will be active to avoid that a glitch on the $\overline{\text{PSON}}$ input may disable/enable the $\overline{\text{FPO}}$ output. When the $\overline{\text{PSON}}$ is set low, the undervoltage function is disabled

during 75ms to avoid turn-on failure. At turn-off, there is an additional delay of 2.3ms from $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$.

Power should be delivered to the rails only when the $\overline{\text{PSON}}$ signal is held at ground potential, thus the $\overline{\text{FPO}}$ becomes a low state after a debounce of 38ms. The $\overline{\text{FPO}}$ pin can be connected to +5V(or up to +15V) through a pull-up resistor.

## Under Voltage Protection(UVP)

The FAN7680 provides undervoltage protection(UVP) for the +3.3V, +5V, and +12V power rails. When an undervoltage condition appears at one of the VS33(+3.3V), VS5(+5V), or Vcc(+12V) input pins for more than 73us, the PGO goes low and $\overline{\text{FPO}}$ output goes high. Also, this fault condition will be latched until the $\overline{\text{PSON}}$ is toggled from low to high or the Vcc falls below a minimum operating voltage.

When the power supply is turned on by the AC input or $\overline{\text{PSON}}$, an internal UVP delay is 75ms. But at normal state an UVP delay time is a 73us debounce time. The need for undervoltage protection is often overlooked in off-line switching power supply system design. But it is very important in battery powered or hand-held equipment since the TTL or CMOS logic often malfunctions under UVP condition.

## Over Voltage Protection(OVP)

The overvoltage protection(OVP) of the FAN7680 monitors +3.3V, +5V, and +12V(the +12V output is sensed via the Vcc pin). When an overvoltage condition appears at one of the +3.3V, +5V, or +12V input pins for more than 73us, the $\overline{\text{FPO}}$ output goes high and the PGO goes low. Also, this fault condition will be latched until the $\overline{\text{PSON}}$ is toggled from low to high or Vcc drops below a minimum operating voltage. During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage to the system. To protect the system under these abnormal conditions, it is common practice to provide overvoltage protection within the power supply.

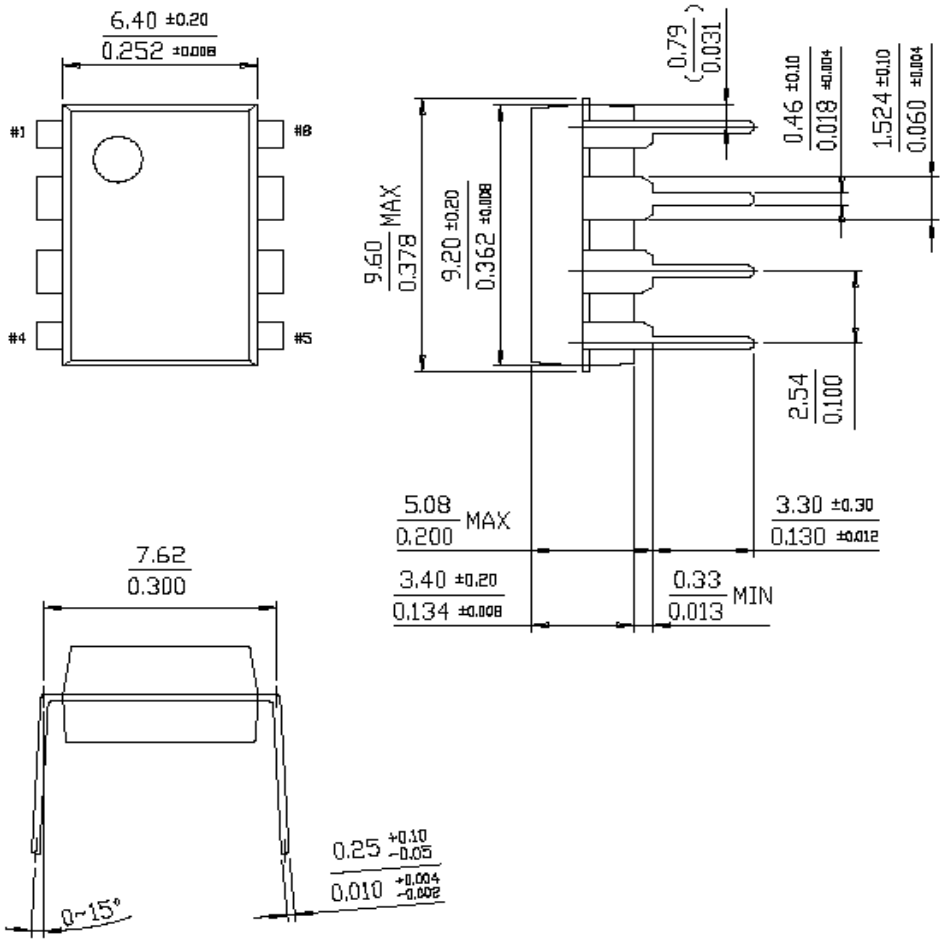
Because TTL and CMOS circuits are very vulnerable to overvoltage, it is becoming industry standard to provide overvoltage protection on all +3.3V, +5V, and +12V outputs. Therefore, not only the +3.3V and +5V rails for the logic circuits on the motherboard need to be protected, but also the +12V peripheral devices such as the hard disk, flopply disk, and CD-ROM players etc., need to be protected.

## Mechanical Dimensions

### Package

**Dimensions in millimeters**

# 8-DIP

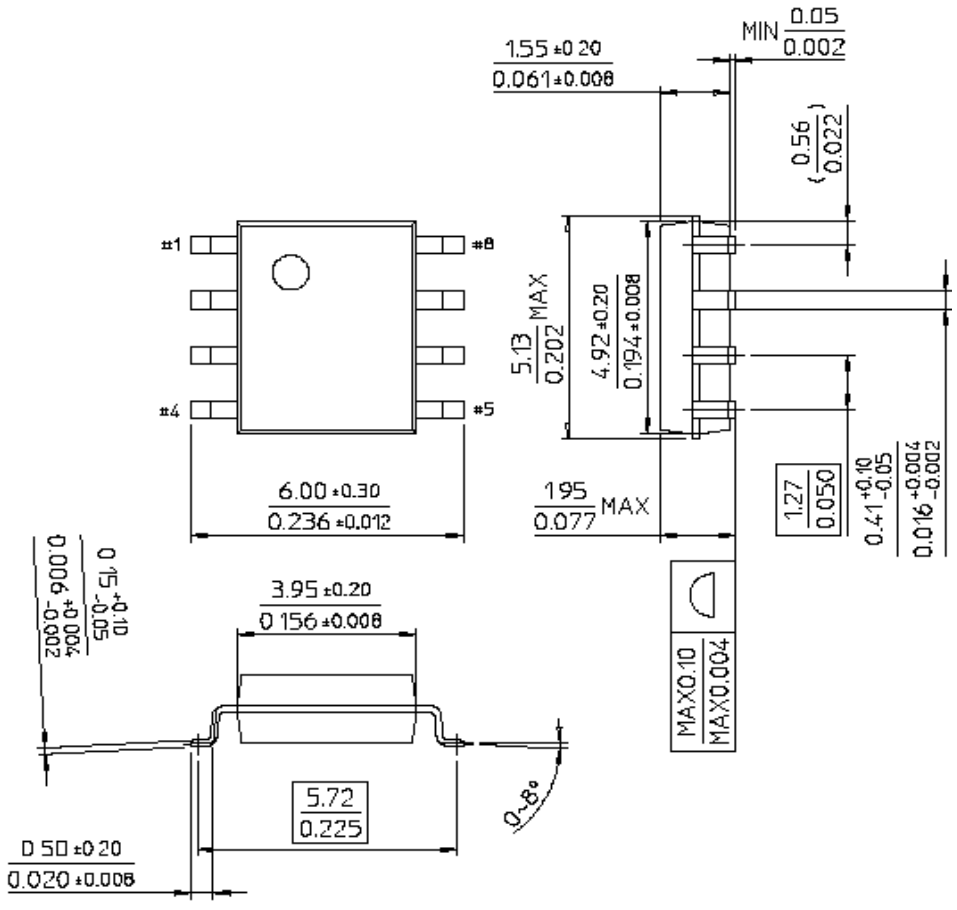


## Mechanical Dimensions

### Package

**Dimensions in millimeters**

# 8-SOP



## Ordering Information

| Product Number | Package | Operating Temperature |
|---|---|---|
| FAN7680N | 8DIP | -40°C ~ +125°C |
| FAN7680M | 8SOP | |

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